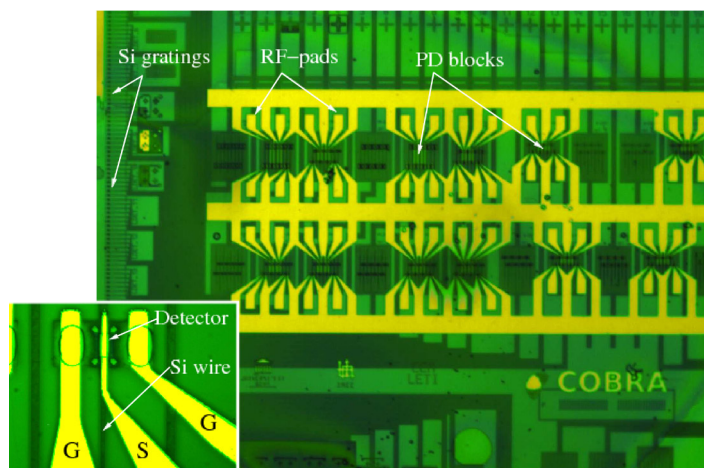


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X. J. M. Leijtens
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J. Van Campenhout
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P. R. A. Binetti,^{1,5} X. J. M. Leijtens,¹ T. de Vries,¹ Y. S. Oei,¹ L. Di Cioccio,²
J.-M. Fedeli,² C. Lagahe,³ J. Van Campenhout,⁴ D. Van Thourhout,⁴
P. J. van Veldhoven,¹ R. Nötzel,¹ and M. K. Smit¹

¹COBRA Research Institute Technische Universiteit Eindhoven, 5600 MB, Eindhoven, The Netherlands

²Commissariat à l'Energie Atomique/Laboratoire d'Electronique de Technologie de l'Information (CEA-LETI), 38054 Grenoble, France

³TRACIT Technologies, 38054 Grenoble, France

⁴Ghent University-Interuniversity Microelectronics Center (IMEC), Department of Information Technology (INTEC), 9000 Gent, Belgium

⁵Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA

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Abstract: We present an InP-based membrane p-i-n photodetector on a silicon-on-insulator sample containing a Si-wiring photonic circuit that is suitable for use in optical interconnections on Si integrated circuits (ICs). The detector mesa footprint is $50\ \mu\text{m}^2$, which is the smallest reported to date for this kind of device, and the junction capacitance is below 10 fF, which allows for high integration density and low dynamic power consumption. The measured detector responsivity and 3-dB bandwidth are 0.45 A/W and 33 GHz, respectively. The device fabrication is compatible with wafer-scale processing steps, guaranteeing compatibility toward future-generation electronic IC processing.

Index Terms: Optical interconnects, photodetector.

1. Introduction

Silicon electronic integrated circuits (ICs) are expected to suffer a bottleneck at the interconnection level as electrical interconnects (EIs) are predicted to limit the maximum bandwidth that can be achieved for both on-chip and off-chip links in future Si ICs [1]. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the complementary metal-oxide-semiconductor (CMOS) circuitry is a promising solution, providing bandwidth increase and reduction in power consumption [2], [3]. A migration from EIs to optical interconnects (OIs) is currently underway for short-reach off-chip applications, such as server backplanes and multitrack machines interconnects [4], and recent studies demonstrate the benefits of photonic ICs for on-chip applications as well [5].

In this paper, we present an InP/InGaAs photodetector (PD) suitable for OIs on electronic ICs. The device is processed on an InP-based layer stack flip-chip bonded on a silicon-on-insulator (SOI) wafer containing Si photonic waveguides. The PD fabrication is compatible with wafer-scale processing steps, to guarantee compatibility with the manufacture of electronic ICs. The potential of the heterogeneous Si/InP technology to integrate optical sources, amplifiers, modulators, and

detectors on CMOS ICs make our approach very appealing for OIs, for which the excellent properties of InP active devices operating at 1550 nm can be combined with Si interconnect waveguides, showing low losses in the C-band [6]. State-of-the-art heterogeneous Si/InP PDs have also been demonstrated by Park *et al.* [7], [8].

We report significant improvements in device size by reducing the PD mesa footprint to $50\ \mu\text{m}^2$, which is the smallest reported to date for these types of detectors, to the best of our knowledge. The compact size keeps the diode capacitance below 10 fF, guaranteeing low dynamic power consumption, and increases the potential for high integration density, which are key parameters for devices used in OIs. This is achieved while keeping fairly high PD efficiency and speed, as discussed in [9]. Such tradeoff is often a limiting factor for PDs realized in different technologies. Implanted Si waveguide detectors are typically millimeter-long due to the low absorption at 1550 nm [10]. Ge PDs are typically shorter ($< 100\ \mu\text{m}$ to hundreds of micrometers for waveguide-detector configurations), the performance is comparable with III–V PDs on Si, and the advantage is that they can be monolithically integrated on a Si substrate, although that requires sophisticated epitaxy techniques to overcome the 4% lattice mismatch between the two materials [11]–[13].

In this paper, we expand on PD design and report on device fabrication and characterization, demonstrating a good match between theoretical expectations and experimental results.

2. Design and Fabrication

The PD structure is defined on top of the bonding layer, as shown in Fig. 1, and consists of two parts: an InP membrane input waveguide meant to couple the light out of the Si photonic wire on the SOI wafer and a p-i-n junction, where the optical power is absorbed. The diode heterojunction is built as a non-intentionally doped 700-nm InGaAs absorbing layer sandwiched between a highly p-doped 50-nm InGaAs contact layer and a highly n-doped 250-nm InP layer, which is also used to realize the membrane waveguide, and has a footprint of $5 \times 10\ \mu\text{m}^2$. We chose a total device thickness of $1\ \mu\text{m}$ to meet a tradeoff between efficiency and speed. In our PD structure, the latter is mostly limited by the photocarrier transit time in the diode depletion region. Calculations outlined by Lucovsky *et al.* [14] were used to predict the transit-time-limited 3-dB cutoff point of the PD frequency response. If assuming that the photocarriers are uniformly generated in the diode intrinsic region, the calculated frequency response for our PD structure is the one plotted in Fig. 2 (curve labeled “uniform illumination”). An absorption layer thickness of 700 nm brings to a predicted 3-dB bandwidth of about 35 GHz. A more accurate analysis should take into account the exponential decay of the light absorbed in the depletion region when illuminated from the n-contact side of the device [14]. Applying the analysis to our PD structure, the frequency response is plotted in Fig. 2 (curve labeled “n-side illumination”), which shows that the expected 3-dB cutoff point is around 30 GHz. The internal quantum efficiency was investigated by calculating the complex slab modes guided by the detector layer stack by applying the scattering matrix approach described by Visser *et al.* [15] and calculating the optical power loss as a function of the propagation length. Simulations show that all the optical power is absorbed within $7\ \mu\text{m}$. However, about 20% of the power is absorbed in the contact layers and in the metal stack. The light absorbed in this region is lost, as it does not contribute to the generated photocurrent. Therefore, a maximum efficiency around 80% is expected.

The detector input InP coupler, which acts as a vertical directional coupler, was designed to achieve mode matching with the Si photonic waveguide, which is 500 nm wide and 220 nm thick (see Fig. 1). We fixed the InP waveguide thickness to 250 nm, which leads to a predicted optimum waveguide width and length of $1\ \mu\text{m}$ and $14\ \mu\text{m}$, respectively, for which simulations show that 100% coupling efficiency is achieved [16]. The PD structure shown in Fig. 1 allows the fabrication of laterally tapered membrane couplers, which provide an increase of the alignment tolerance between the waveguides without additional processing steps. Further details about the Si photonic waveguides were presented in [17]. The PD layer stack described in the previous section was grown on a 2" InP wafer. The wafer was sawn in dies that were then bonded upside down on a processed SOI wafer containing the Si waveguides by means of direct molecular bonding, using a

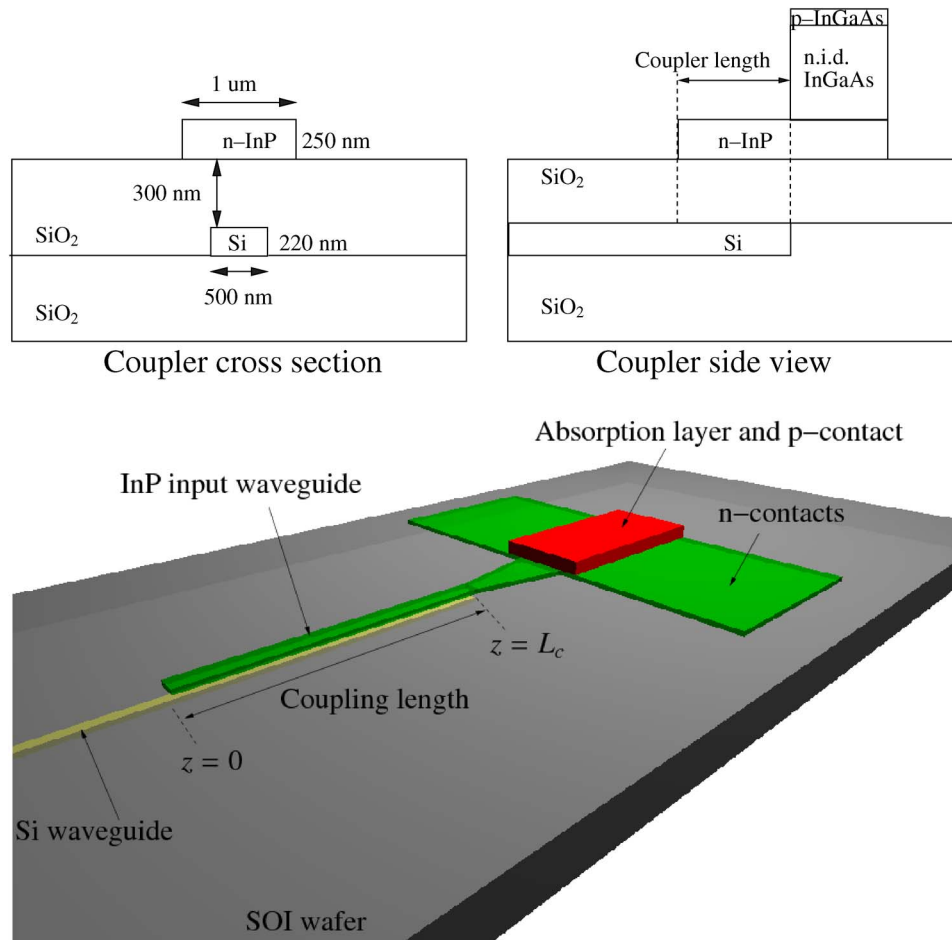


Fig. 1. PD structure. The coupling from the Si photonic waveguide layer to the PD is realized through the InP membrane input waveguide, on top of which the detector is stacked.

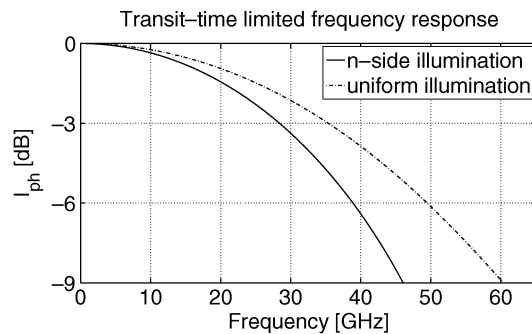


Fig. 2. Transit-time-limited frequency response of the p-i-n photodiode calculated as a function of the type of device illumination. The calculations were made for an absorption layer thickness of 700 nm. These curves were generated by using [14, Eqs. (37) and (52)].

300-nm-thick SiO₂ interface [18]. The PDs were defined via a combination of wet-etching and dry-etching steps, as we describe in [19]. Fiber grating couplers (FGCs) were also integrated into the Si photonic waveguide layer for fiber-to-waveguide light coupling, which is necessary for the

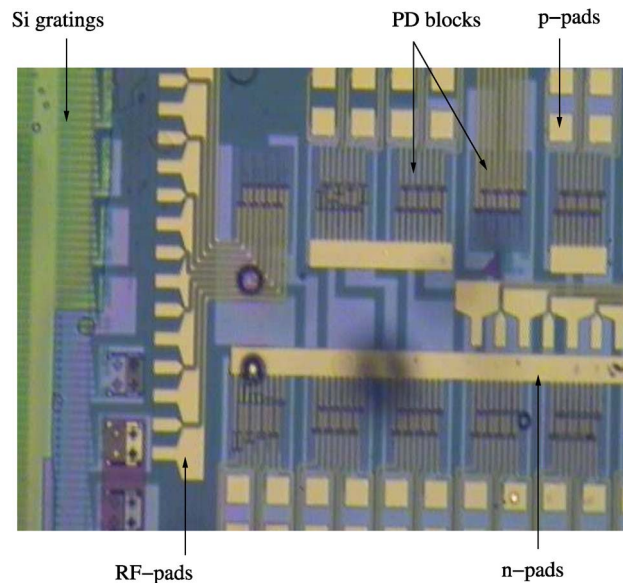


Fig. 3. Chip picture. The PDs are grouped in blocks of 8, where some are contacted with DC pads. Metal coplanar waveguides interconnect the RF pads to the diode contact layers. The Si FGCs used for fiber-to-waveguide light coupling are also indicated.

characterization of detectors. Such gratings can be seen in the left part of Fig. 3, which shows a picture of the fabricated devices. A detailed description about the FGCs can be found in [20].

3. Measurement Results

The device DC characterization was performed by using a tunable laser source (TLS) to illuminate the Si waveguide that leads to the detector and a Keithley 2400 current/voltage source meter unit to reversely bias the PD and to read out the generated photocurrent. First, the detector dark current at different applied bias voltages was measured. Dark currents around 1.6 nA were registered at -4 V. A TLS and a polarization controller were used to couple 1550-nm light into the Si waveguide via the Si FGC, which is designed to work with TE-polarized light [21]. The photodiode-generated photocurrent as a function of the applied bias voltage was measured for the following TLS output powers: 0 mW, 0.2 mW, and 0.4 mW.

On-chip test structures were used to measure a 20% maximum coupling efficiency of the Si FGC at 1575 nm and 4–5-dB/cm propagation loss of the 500×220 nm² Si waveguides at 1550 nm. Taking into account 0.7-dB loss due to the fiber connections from the TLS to the polarization controller, the detector optical input powers corresponding to the TLS intensities mentioned above are 0 μ W, 25 μ W, and 50 μ W. The PD responsivity was thus calculated to be $R = 0.45$ A/W, which is a conservative value, as the FGC maximum efficiency was assumed. Such responsivity corresponds to a quantum efficiency $\eta = 35\%$, which includes the internal quantum efficiency of the pin detector and the efficiency of the InP membrane coupler. This result is consistent with the expected diode internal quantum efficiency and the measured 50% efficiency of the coupler we previously reported [16]. Measurement results are shown in Fig. 4, which also demonstrates the linear response of the PD to the incoming input power. Residual ripples might be attributed to optical power reflections between the probing fiber and the chip and mechanical instabilities of the measurement setup. Optical-to-Electrical dynamic measurements of the PDs were performed in the range of 100 MHz to 40 GHz with an Agilent HPN4373B 67-GHz lightwave component analyzer (LCA). The LCA optical module was used for modulating the optical power from the 1550-nm laser source integrated in the LCA. The modulated optical signal was amplified with an erbium-doped fiber amplifier and a 1.5-nm pass-band filter was employed to improve the signal-to-noise ratio. The

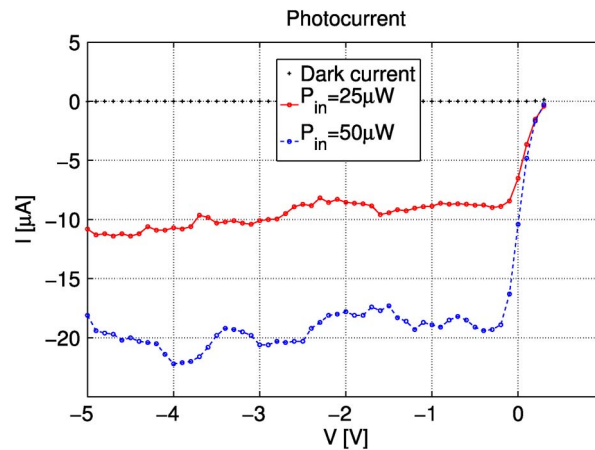


Fig. 4. Measured photocurrent for 0- μ W, 25- μ W, and 50- μ W optical input power as a function of the detector applied bias voltage.

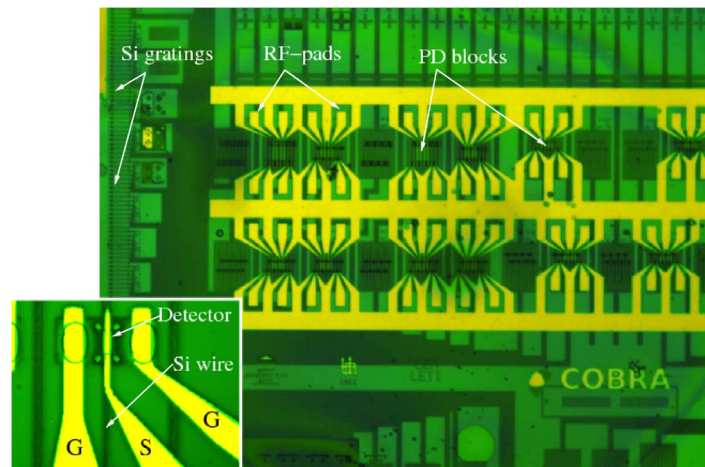


Fig. 5. Picture of the fabricated detectors with improved metallization pattern. A close-up of a detector is shown in the inset.

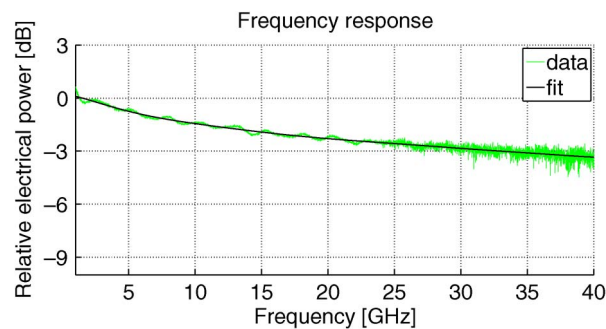


Fig. 6. Detector RF frequency response.

electrical input port of the LCA was used for reading out the RF photogenerated electrical signal, while the average photocurrent was monitored with a Keithley 2400 unit, which was also employed for fiber-to-waveguide alignment and photodiode reverse DC biasing. The frequency response of the

RF cables, RF adaptors, bias-tee and RF probe was deembedded through the LCA calibration. The detector structures shown in Fig. 3 showed a frequency response 3-dB cutoff point below 15 GHz, limited by the parasitic capacitance of the 1–1.5-mm-long metal coplanar waveguide structure interconnecting the RF pads to the diode contact layers. This issue was tackled in a following chip run, in which the RF pads were defined close to the devices and connected to the contact layers by means of 100- μm -long tapers, as shown in Fig. 5. Results are presented in Fig. 6. A 3-dB cutoff frequency response of about 33 GHz was measured, which quite well matches the expectations.

4. Conclusion

We presented an InP-based PD fabricated on a bonded SOI wafer containing Si waveguides. The device is the smallest reported to date, with a mesa footprint of 50 μm^2 and a junction capacitance below 10 fF. This makes the device suitable for OIs on Si ICs, allowing for high integration density and low dynamic power consumption. Measured detector responsivity and 3-dB bandwidth are 0.45 A/W and 33 GHz, respectively.

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